**Course Title: Digital Logic and System Design**

**Course Code: CSE 210**

**Credit Hour: 1.5**

**Experiment No. 4**

**Experiment Name:**

**a) Design 1 bit Half Adder and Full Adder**

**b) Test and verify the 4-bit parallel Adder(IC # 7483)**

**c) Design Subtractor using IC # 7483**

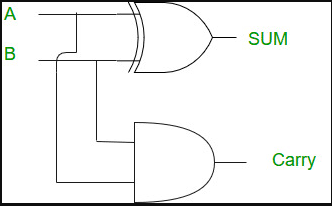
**d) Adder + Subtractor**

**e) Design a 4 bit adder-subtractor with full adders.**

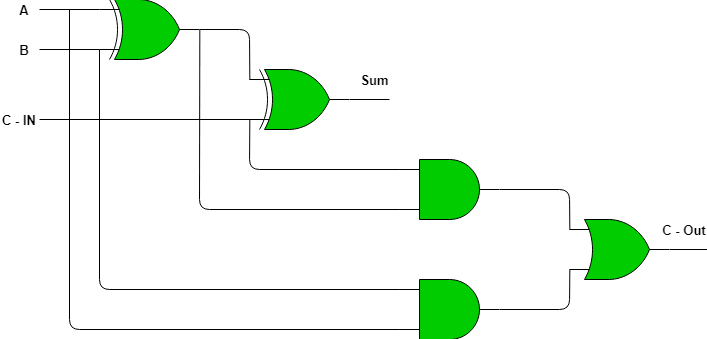
**Tasks:**

**a) Design a Half adder and Full adder:**

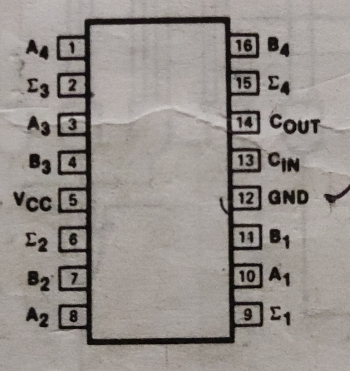
Half adder:

Image result for half adder"

Full adder: A -1



**b) Test and verify the 4-bit parallel Adder(IC # 7483)**

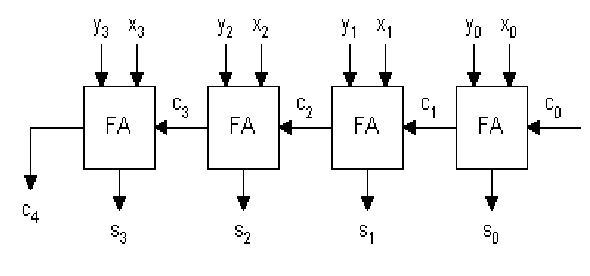




**c) Design Subtractor using IC # 7483**

Use (i) Not gate (ii) Xor Gate

**(e) Design a 4 bit adder-subtractor with full adders**



**Report:** 1) Problem Statement

2) Instruments (used in this experiment)

3) Truth Table

4) Logic expression

5) Logic diagram

6) 4 – bit example of Adder and Substractor

7) Discussion